REMARKS

Claims 1-9, 11-19, 21-27, 29, and 31-37 are pending in this application. No amendments to the claims are made by this Response. Reconsideration of the claims in view of the following remarks is respectfully requested.

I. Telephone Interview

Applicants thank Examiner Parthasarathy for the courtesies extended to Applicants' representative during the December 5, 2007 telephone interview. During the telephone interview, the above amendments and the distinctions of the claims over the cited art were discussed. Examiner Parthasarathy indicated her understanding of Applicants' position with regard to each of the rejections set forth in the Final Office Action being in error and requested that Applicants file a formal response with Applicants' arguments to place them in the record. Specifically, Examiner Parthasarathy indicated that the confusion that led to each of the rejections is where in the specification the features of an isolated state, a shared state, a control processor, and a controlled processor are described. Examiner Parthasarathy requested that Applicants point to exemplary portions of the specification showing where these features are supported. The substance of the telephone interview is summarized in the following remarks.

II. Finality of the Office Action Improper

Applicants respectfully submit that the finality of the Office Action mailed October 30, 2007 is improper since the rejections set forth in the Office Action were not necessitated by Applicants' amendments to the claims made in the Response filed July 5, 2007. In particular, the Final Office Action includes an obviousness-type double patenting rejection that was not present in the First Office Action. Moreover, Applicants' amendments to the claims to insert the word "controlled" prior to processor did not suddenly cause the issue of obviousness-type double patenting to be raised. Thus, Applicants' amendments did not necessitate the new basis for rejection and hence, the

Final Office Action includes a rejection that was not necessitated by amendment. A Final Office Action cannot be made final simply because some changes to the rejections were necessitated by amendment and others were not. To the contrary, if even one rejection is changed and that change was not necessitated by Applicants' amendments then the Office Action as a whole must be made non-final. For these reasons, Applicants respectfully submit that the finality of the Final Office Action should be withdrawn.

III. Response to Examiner's Request to Cite Specification for Support of Claimed Features

In response to Examiner Parthasarathy's request during the December 5, 2007 telephone interview, Applicants will hereby provide citations to the specification where the features of an isolated state, a shared state, a control processor, and a controlled processor are described with regard to illustrative embodiments. These citations will be made with regard to paragraph numbers of the corresponding U.S. Patent Application Publication 2005/0071651 in order to make it easier for the Examiner to locate these sections of the application.

It should be appreciated that these citations are made only for the edification of the Examiner with regard to illustrative embodiments and are not intended, and should not be construed, to be limiting on the features of the claims. To the contrary, the illustrative embodiments are only exemplary of the many different possible embodiments that are within the scope of the claims and thus, are not limiting on the claims. Applicants do not intend to further limit the claims in any way by the following citations to the specification.

During the December 5, 2007 telephone interview, Examiner Parthasarathy requested that Applicants identify where in the specification there is support for the features of a "control processor" and a "controlled processor." Applicants respectfully direct the Examiner's attention to Figure 2 and paragraph [0075] of the present application. In this section of the specification it is explicitly stated, with regard to the illustrative embodiment depicted in Figure 2, that "under the control of PU 203, the SPUs perform the processing of these data and applications in a parallel and independent

manner." Thus, the PU is a control processor while the SPUs are controlled processors. This is one example of an architecture in which a control processor and controlled processors may be provided. Therefore, the specification provides support at least in paragraph [0075] and Figure 2 for the use of the terms "control processor" and "controlled processor" in the present claims with at least this example illustrative embodiment.

In addition, during the telephone interview, Examiner Parthasarathy requested that Applicants identify where in the specification there is support for the features of an "isolated state" and a "shared state." Applicants respectfully direct the Examiner's attention to Figure 57 and paragraphs [0200]-[0201]. Figure 57 shows an example of utilizing one SPU in an isolated state (the encryption SPU 5730 in the private mode) while the other SPUs are in a shared state (SPUs 5760 in shared mode). Furthermore, paragraphs [0200]-[0201] read:

> FIG. 57 is a system diagram showing the system components and intercommunication involved in using one of the SPUs as an isolated encryption device. When an SPU is set up as an encryption device, its local memory is not shared in the common memory map. So, while the encryption SPU can read and write data to and from shared common memory (i.e., using DMA commands), other processors are unable to read and write to the encryption SPU's local memory. In addition, special, nonvolatile registers that can be used to store a variety of encryption keys is available to the encryption SPU, however these special registers cannot be read by SPUs that are operating in "shared" mode (i.e., special registers are not available to SPUs that have local memory mapped to the shared memory map).
>
> Common memory map 5710 shows memory that is shared amongst the processors. In one embodiment, each SPU and PU has its own DMA controller for accessing shared memory. Common (shared) memory includes PU local memory 5715 as well as shared local memory 5720 of those SPUs (5760) that are running in shared, as opposed to private, mode. In the example shown in FIG. 57, SPU local memory 5765 is mapped to common memory map 5710 as shared memory 5720. As shared memory, other processors, such as PU 5700, are able to read and write data to local memory of SPUs that are running in shared mode.
> (emphasis added)

Thus, the figures and the specification, at least at these cited sections, clearly provide support for an isolated state (or private mode) and a shared state (or shared mode) of processors. Again, this is only one exemplary illustrative embodiment.

Turning now to the actual rejections set forth in the Office Action, Applicants will first address the rejections under 35 U.S.C. § 112 since it was stated by the Examiner during the telephone interview that Applicants' clarification in response to these rejections would also address the issues raised in the double patenting rejection and rejection under 35 U.S.C. § 101.

IV. Rejection under 35 U.S.C. § 112, First Paragraph

The Final Office Action rejects claims 1-9, 11-19, 21-27, 29, and 31-37 under 35 U.S.C. §112, first paragraph as allegedly failing to comply with the written description requirement. Specifically, the Office Action alleges that the specification does not recite "controlled" processors. Applicants respectfully disagree.

As set forth above, at least in Figure 2 and in paragraph [0075], the present specification provides support for a control processor, such as the PU 203, and a plurality of controlled processors, such as SPUs 203 and 207-221. There is further ample support throughout the specification regarding SPUs being controlled processors and PUs being control processors. While the term "controlled processors" and "control processor" itself may not be explicitly used within the specification, there is support for these terms in the very exemplary illustrative embodiments described in the specification. One of ordinary skill in the art would readily understand that a "control processor" is a processor that controls the operation of other processors while a "controlled processor" is a processor whose operation is controlled by another processor. This is precisely what the exemplary illustrative embodiments describe when describing the PU as controlling the SPUs.

In view of the above, Applicants respectfully submit that the present specification provides a written description that reasonably conveys to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Thus, Applicants respectfully request withdrawal of the rejection of claims 1-9, 11-19, 21-27, 29, and 31-37 under 35 U.S.C. §112, first paragraph.

V. Rejection under 35 U.S.C. § 112, Second Paragraph

The Final Office Action rejects claims 1-9, 11-19, 21-27, 29, and 31-37 under 35 U.S.C. §112, second paragraph as allegedly being indefinite. In the December 5, 2007 telephone interview, the Examiner explained that this rejection is made under the same alleged basis as the rejection under 35 U.S.C. § 112, first paragraph rejection. Applicants have shown above where there is support for the features of a "control processor" and "at least one controlled processor." Furthermore, Applicants have shown above where there is support for the "shared operational state" and the "isolated operational state" of the processors. Thus, the Examiner's alleged basis for holding the claims indefinite is in error.

Moreover, alleging that there is no support for features in a claim is not a proper basis for a rejection under 35 U.S.C. § 112, second paragraph. The second paragraph of 35 U.S.C. § 112 is directed to the specificity of the terminology used in the claim itself and whether it apprises one of ordinary skill in the art of the scope of the subject matter sought to be patented, not whether the features of the claims are supported by the description in the application (this is properly rejected under 35 U.S.C. § 112, first paragraph, as addressed above). There is no indefiniteness in the terminology used in any of the pending claims. Thus, the claims are not indefinite under 35 U.S.C. § 112, second paragraph, despite the allegations raised in the Final Office Action. Accordingly, Applicants respectfully request withdrawal of the rejection under 35 U.S.C. § 112, second paragraph.

VI. Rejection under 35 U.S.C. § 101

The Final Office Action rejects claims 1-9, 11-19, 21-27, 29, and 31-37 as allegedly being directed to non-statutory subject matter. Specifically, the Final Office Action alleges that independent claims 31-33 are not limited to tangible embodiments. Applicants respectfully disagree.

First, it should be noted that claim 32 is a system claim that is clearly recited as comprising a control processor, a plurality of controlled processors, and a common

memory. These are all physical devices and thus, cannot possibly be considered to be "intangible." Thus, claim 32 is clearly directed to a "tangible embodiment," contrary to the allegations made in the Final Office Action.

Claim 31 reads as follows:

> 31. A method, in a multiprocessor system, the multiprocessor system comprising a control processor and a plurality of controlled processors, the method comprising:
>
> selecting at least one controlled processor of the plurality of controlled processors to operate in a shared operational state;
>
> selecting a second controlled processor from the plurality of controlled processors to operate in an isolated operational state;
>
> configuring the at least one first controlled processor of the multiprocessor system to be in the shared operational state, wherein the shared operational state causes the at least one first controlled processor to operate using a common memory accessible by the plurality of controlled processors in the multiprocessor system;
>
> configuring the second controlled processor of the multiprocessor system, via loading and executing initialization code in the second controlled processor, to be in the isolated operational state, wherein the isolated operational state causes a local memory associated with the second controlled processor to be not accessible by the at least one first controlled processor;
>
> executing first code within the second controlled processor in a secure manner by virtue of the isolated operational state; and
>
> executing second code within the at least one first controlled processor in an unsecured manner by virtue of the shared operational state. (emphasis added)

Thus, claim 31 is a method claim in which the method is implemented in a "multiprocessor system." The method comprises operations including configuring at least one first controlled processor to be in a shared operational state and configuring a second controlled processor to be in an isolated operational state. The method further comprises operations for executing code within the second controlled processor in a secure manner by virtue of the isolated operational state and executing code within the at least one first controlled processor in an unsecured manner by virtue of the shared operational state. Thus, the configuring operations in claim 31 tangibly change the multiprocessor system and the operation of the multiprocessor system. That is, prior to the configuring operations in the method of claim 31, the controlled processors of the

multiprocessor system would not specifically operate such that one controlled processor was isolated from the other controlled processors. Hence, a tangible result is achieved by the operation of the method of claim 31 in that the processors function differently than before.

Thus, contrary to the allegations raised in the Final Office Action, claim 31 does recite a tangible embodiment and therefore, is directed to statutory subject matter. Similar considerations apply to claim 32 which is a computer program product claim but which also recites such operations for configuring processors in a multiprocessor system and executing code on the configured processors. Therefore, in view of the above, Applicants respectfully request withdrawal of the rejection of claims 1-9, 11-19, 21-27, 29, and 31-37 under 35 U.S.C. § 101.

VII. Obviousness Type Double Patenting Rejection

The Final Office Action rejects claims 1-9, 11-19, 21-27, 29, and 31-37 on the ground of non-statutory obviousness type double patenting as being allegedly unpatentable over claims 1-24 of U.S. Patent No. 6,981,072. This rejection is respectfully traversed.

The improper nature of this rejection can be clearly seen from a simple comparison of the independent claims in the present application with those of the '072 patent. For example, taking the independent system claim of the present application, i.e. claim 32, and the independent system claim of the '072 patent, i.e. claim 1, the following comparison can be made where differences between the present application and the '072 patent are illustrated by underline emphasis:

Present Application	U.S. Patent No. 6,981,072
32. An information handling system, comprising: a control processor; a plurality of controlled processors, wherein each of the plurality of controlled processors comprises a local memory; and a common memory shared by the control processor and the plurality of controlled processors in the information handling system, wherein the plurality of controlled processors comprises: at least one first controlled processor selected and configured to be in a shared operational state, wherein the shared operation state causes the at least one first controlled processor to operate using the common memory; and a second controlled processor selected and configured, via loading and executing initialization code in the second controlled processor, to be in an isolated operational state, wherein the isolated operational state causes a local memory associated with the second controlled processor to be not accessible by the at least one first controlled processor, wherein the second controlled processor executes first code in a secure manner by virtue of the isolated operational state, and wherein the at least one first controlled processor executes in an unsecured manner by virtue of the shared operational state.	1. A non-homogeneous, asymmetric multiprocessor system, comprising: a general-purpose processor; a special-purpose processor; a first memory management unit (MMU) coupled to the general-purpose processor to translate an effective address received from the general-purpose processor into a first physical address; a direct memory access controller (DMAC) coupled to the special-purpose processor to translate a DMA command received from the special-purpose processor into an address; a second MMU coupled to the DMAC to translate the address into a second physical address; and a system memory coupled to both the first and second MMUs, wherein the system memory is accessed by the general-purpose processor and the special-purpose processor via the first and second physical addresses respectively.

As can be clearly seen from the above comparison, the present claim 32 does not include the features of a first MMU, a second MMU, the DMAC, a system memory being coupled to the first and second MMUs, or the specific couplings of elements set forth in claim 1 of the '072 patent. Moreover, the '072 patent does not teach or suggest a plurality of controlled processors (only a general purpose processor and a special purpose processor are recited), a shared operational state, an isolated operational state, particular controlled processors being configured to operate in respective ones of the shared operational state and isolated operational state, or executing code in a secure manner or

unsecure manner by virtue of the isolated operational state or shared operational state as recited in claim 32 of the present application. Moreover, these features are not obvious in view of the claims of the '072 patent since none of the claims recite any such features and there is no other art cited by the Examiner that teaches or suggests such features.

A similar comparison may be made with each of the independent claims of the present application and corresponding claims in the '072 patent with each comparison clearly showing how the claims of the present application are not obviated by the claims of the '072 patent. Thus, Applicants respectfully submit that claims 1-9, 11-19, 21-27, 29, and 31-37 are improperly rejected on the ground of non-statutory obviousness type double patenting as being allegedly unpatentable over claims 1-24 of U.S. Patent No. 6,981,072 and respectfully request that this rejection be withdrawn.

VIII. Conclusion

It is respectfully urged that the subject application is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,

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